REMARKS

The Examiner is thanked for the thorough examination and search of the subject.

Claims 43-74, 83, 84 and 89-102 are pending; Claims 43, 48, 51, 57-59, 64, 69, 72, 83, 89, 94 and 97 have been currently amended; Claims 1-42, 75-82 and 85-88 have been canceled. No new matter is believed to have been added.

Response to Claim Rejections under 35 U.S.C. 102 and 103

Applicant respectfully traverses the rejections for at least the reasons set forth below.

Response to Claims 43-63

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As currently amended, independent Claim 43 is recited below:

43. A chip structure comprising:

a silicon substrate;

a resistor in said silicon substrate, wherein said resistor comprises silicon with a dopant;

a MOS device comprising a portion in said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a first dielectric layer between said first and second metal layers;

a passivation layer over said metallization structure and over said first dielectric layer, wherein a first opening in said passivation layer is over a first

contact point of said metallization structure, and said first contact point is at a bottom of said first opening, and wherein a second opening in said passivation layer is over a second contact point of said metallization structure, and said second contact point is at a bottom of said second opening, wherein said first and second contact points are separated from each other by an insulating material, wherein said passivation layer comprises an insulating nitride layer; and

a circuit trace over said passivation layer and over said first and second contact points, wherein said first contact point is connected to said second contact point through said circuit trace, and wherein said circuit trace is connected to said resistor through said first opening.

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Reconsiderations of Claims 43 and 48-53 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (U.S. Pat. No. 6,495,442) in view of Woolery et al. (U.S. Pat. No. 6,528,380), of Claims 54-56 and 59 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al. and Erdejac et al. (U.S. Pat. No. 6,235,101), of Claims 57 and 60-63 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al. and Carichner et al. (U.S. Pat. No. 5,972,734) or over Lin et al. in view of Woolery et al., Erdejac et al. and Carichner et al., of Claims 44-46 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al., further in view of Leidy (U.S. Pub. No. 2003/0155570), and of Claims 45 and 47 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al., further in view of Simila (U.S. Pub. No. 2003/0183332) are requested in accordance with the following remarks.

Applicant respectfully asserts that the chip structure currently claimed in Claim 43 patentably distinguishes over the citations by Lin et al. (U.S. Pat. No. 6,495,442) in view of Woolery et al. (U.S. Pat. No. 6,528,380).

The Examiner considers that Lin et al.'s chip structure comprises a resistor in a silicon substrate (not shown but "transistors and other devices" is described in col. 4, lines 49-51). *~ See lines 13-16 on page 2, in the last Office Action mailed Jun. 27, 2008 ~* Furthermore, the Examiner considers that "Lin discloses there are "transistors and other devices" in the silicon substrate and one of ordinary skill in the art at the time the invention was made would interpret this disclosure to include resistors." *~ See lines 13-15 on page 12, in the last Office Action mailed Jun. 27, 2008 ~*

Applicant respectfully traverses the Examiner's opinion because interpretation of "transistors and other devices" to "the disclosure including a resistor" is improper. Lin et al. fail to teach what kind of other devices could be, and thus the wording of "transistors and other devices" can not be deemed as the disclosure including a resistor.

Also, Lin et al. fail to teach, hint or suggest the subject matter, currently claimed in Claim 43, that a circuit trace over a passivation layer may be connected to a resistor in a silicon substrate, not as described by the Examiner in lines 9-17 on page 3, in the last Office Action mailed Jun. 27, 2008.

Withdrawal of rejection under 35 U.S.C.103(a) to Claim 43 is respectfully requested.

For at least the foregoing reasons, applicant respectfully submits independent Claim 43 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 44-63 patently define over the prior art as well.

Response to Claims 64-74, 83 and 84

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As currently amended, independent Claim 64 is recited below:

64. A chip structure comprising:

a silicon substrate;

a resistor in said silicon substrate, wherein said resistor comprises silicon with a dopant;

a MOS device comprising a portion in said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a dielectric layer between said first and second metal layers;

a passivation layer over said metallization structure and over said dielectric layer, wherein a first opening in said passivation layer is over a first contact point of said metallization structure, and said first contact point is at a bottom of said first opening, and wherein a second opening in said passivation layer is over a second contact point of said metallization structure, and said second contact point is at a bottom of said second opening, wherein said first and second contact points are separated from each other by an insulating material, wherein said passivation layer comprises an insulating nitride layer; and

a circuit trace over said passivation layer and over said first and second contact points, wherein said first contact point is connected to said second contact point through said circuit trace, wherein said circuit trace is connected to said resistor through said first opening, and wherein said circuit trace comprises a titanium-containing layer and a gold layer over said titanium-containing layer.

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Reconsiderations of Claims 64, 69-74 and 83 rejected under 35 U.S.C. 103(a) as

being unpatentable over Lin et al. (U.S. Pat. No. 6,495,442) in view of Woolery et al. (U.S. Pat. No. 6,528,380) and Carichner et al. (U.S. Pat. No. 5,972,734) or over Lin et al. in view of Woolery et al., Erdejac et al. (U.S. Pat. No. 6,235,101) and Carichner et al., of Claim 84 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al. and Carichner et al., further in view of Yamada et al. (U.S. Pub. No. 2002/0047210), of Claims 65-67 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al., further in view of Leidy (U.S. Pub. No. 2003/0155570), and of Claims 66 and 68 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al., further in view of Simila (U.S. Pub. No. 2003/0183332) are requested in accordance with the following remarks.

Applicant respectfully asserts that the chip structure currently claimed in Claim 64 patentably distinguishes over the citations by Lin et al. (U.S. Pat. No. 6,495,442) in view of Woolery et al. (U.S. Pat. No. 6,528,380) and Carichner et al. (U.S. Pat. No. 5,972,734).

The Examiner considers that Lin et al.'s chip structure comprises a resistor in a silicon substrate (not shown but "transistors and other devices" is described in col. 4, lines 49-51). ~ *See lines 10-13 on page 7, in the last Office Action mailed Jun. 27, 2008* ~ Furthermore, the Examiner considers that "Lin discloses there are "transistors and other devices" in the silicon substrate and one of ordinary skill in the art at the time the invention was made would interpret this disclosure to include resistors." ~ *See lines 13-15 on page 12, in the last Office Action mailed Jun. 27, 2008* ~

Applicant respectfully traverses the Examiner's opinion because interpretation of "transistors and other devices" to "the disclosure including a resistor" is improper. Lin et al. fail to teach what kind of other devices could be, and thus the wording of "transistors and other devices" can not be deemed as the disclosure including a resistor.

Also, Lin et al. fail to teach, hint or suggest the subject matter, currently claimed in Claim 64, that a circuit trace over a passivation layer may be connected to a resistor in a silicon substrate, not as described by the Examiner in lines 10-18 on page 8, in the last Office Action mailed Jun. 27, 2008.

The Examiner considers that "Carichner teaches a circuit trace (212) comprises a titanium-containing layer and a gold layer over said titanium-containing layer (col. 4, lines 41-46)." *~ See lines 5-7 on page 9, in the last Office Action mailed Jun. 27, 2008 ~*

Applicant respectfully traverses the Examiner's opinion because Charichner et al. fail to teach, hint or suggest that a circuit trace may comprise a titanium-containing layer and a gold layer over said titanium-containing layer, as currently claimed in Claim 64. In col. 4, lines 42-46, Charichner et al. teach that "The traces 212 are formed of any conductive material, for example copper, copper-molybdenum-copper or copper-tungsten-copper laminates, beryllium-oxide, or aluminum-nitride metallized with gold alloys or chromium, titanium or nickel", but fail to teach, hint or suggest that a circuit trace may comprise a titanium-containing layer and a gold layer over the titanium-containing layer, as currently claimed in Claim 64. All of Lin et al., Woolery et al. and Carichner et al. are believed to fail to teach, hint or suggest the claimed subject matter that a circuit trace comprises a titanium-containing layer and a gold layer over the titanium-containing layer, as currently claimed in Claim 64.

Withdrawal of rejection under 35 U.S.C.103(a) to Claim 64 is respectfully requested.

For at least the foregoing reasons, applicant respectfully submits independent Claim 64 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 65-74, 83 and 84 patently define over the

prior art as well.

Response to Claims 89-102

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As currently amended, independent Claim 89 is recited below:

89. A chip structure comprising:

a silicon substrate;

a resistor in said silicon substrate, wherein said resistor comprises silicon with a dopant;

a MOS device comprising a portion in said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a dielectric layer between said first and second metal layers;

a passivation layer over said metallization structure and over said dielectric layer, wherein a first opening in said passivation layer is over a first contact point of said metallization structure, and said first contact point is at a bottom of said first opening, and wherein a second opening in said passivation layer is over a second contact point of said metallization structure, and said second contact point is at a bottom of said second opening, wherein said first and second contact points are separated from each other by an insulating material, wherein said passivation layer comprises an insulating nitride layer; and

a circuit trace over said passivation layer and over said first and second contact points, wherein said first contact point is connected to said second contact point through said circuit trace, wherein said circuit trace is connected to said resistor through said first opening, and wherein said circuit trace comprises a copper layer.

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Reconsiderations of Claims 89 and 94-99 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (U.S. Pat. No. 6,495,442) in view of Woolery et al. (U.S. Pat. No. 6,528,380), of Claims 100 and 101 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al. and Carichner et al. (U.S. Pat. No. 5,972,734) or over Lin et al. in view of Woolery et al., Erdejac et al. (U.S. Pat. No. 6,235,101) and Carichner et al., of Claim 102 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al., further in view of Yamada et al. (U.S. Pub. No. 2002/0047210), of Claims 90-92 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al., further in view of Leidy (U.S. Pub. No. 2003/0155570), and of Claims 91 and 93 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al., further in view of Simila (U.S. Pub. No. 2003/0183332) are requested in accordance with the following remarks.

Applicant respectfully asserts that the chip structure currently claimed in Claim 89 patentably distinguishes over the citations by Lin et al. (U.S. Pat. No. 6,495,442) in view of Woolery et al. (U.S. Pat. No. 6,528,380).

The Examiner considers that Lin et al.'s chip structure comprises a resistor in a silicon substrate (not shown but "transistors and other devices" is described in col. 4, lines 49-51). ~ *See lines 3-6 on page 4, in the last Office Action mailed Jun. 27, 2008* ~ Furthermore, the Examiner considers that "Lin discloses there are "transistors and other devices" in the silicon substrate and one of ordinary skill in the art at the time the invention was made would interpret this disclosure to include resistors." ~ *See lines 13-15 on page 12, in the last Office Action mailed Jun. 27, 2008* ~

Applicant respectfully traverses the Examiner's opinion because interpretation of

"transistors and other devices" to "the disclosure including a resistor" is improper. Lin et al. fail to teach what kind of other devices could be, and thus the wording of "transistors and other devices" can not be deemed as the disclosure including a resistor.

Also, Lin et al. fail to teach, hint or suggest the subject matter, currently claimed in Claim 89, that a circuit trace over a passivation layer may be connected to a resistor in a silicon substrate, not as described by the Examiner in lines 1-11 on page 5, in the last Office Action mailed Jun. 27, 2008.

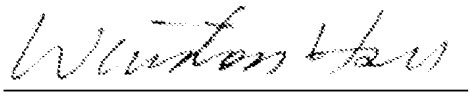
Withdrawal of rejection under 35 U.S.C.103(a) to Claim 89 is respectfully requested.

For at least the foregoing reasons, applicant respectfully submits independent Claim 89 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 90-102 patently define over the prior art as well.

Conclusion

Some or all Claims are believed to be in condition for Allowance, and that is so requested.

Sincerely yours,



Date: 09.25.2008

Winston Hsu, Patent Agent No. 41,526
P.O. BOX 506, Merrifield, VA 22116, U.S.A.
Voice Mail: 302-729-1562
Facsimile: 806-498-6673
e-mail : winstonhsu@naipo.com

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